Electronic Version
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Claims

[c1] 9. A method of fabricating a self-aligned split gate flash cell, comprising:
forming a deep well of a first conductivity type in a substrate;
forming a shallow well of a second conductivity type in the deep well;
forming a gate oxide layer on the substrate;
forming a control gate on the gate oxide layer, wherein a capping layer is disposed on the control gate ,and the capping layer and the control gate form a stacked structure;
forming a tunnel oxide layer on sidewalls of the control gate and the substrate;
forming a conformal conducting layer covering the capping layer and the substrate;
etching back the conformal conducting layer to form a conductivity spacer on the tunnel oxide located on sidewalls of the capping layer and the control gate;
removing the conductivity spacer on one side of the control gate to leave the conductivity spacer on the other side serving as a floating gate;
forming a drain and a common source beneath each side

of the stacked structure in the substrate, wherein the depth of the drain and the common source are larger than the depth of the shallow well of the second conductivity type; and

forming a pocket well of the second conductivity type in the substrate around the drain.

[c2] 10. The method of claim 9, wherein the deep well is an n-type deep well, the shallow well is a shallow p-type well and the pocket well is a p-type well.

[c3] 11. The method of claim 9, wherein the drain and the common source are n^+ doped regions, and the deep well of the first conductivity type is an n^- doped region.

[c4] 12. The method of claim 9, wherein the tunnel oxide layer between the control gate and the floating gate is thicker than the tunnel oxide layer between the floating gate and the substrate.

[c5] 13. The method of claim 9, wherein forming the control gate and the capping layer comprises:

forming a conducting layer and a capping material layer on the gate oxide;

patterning the capping material layer to form the capping layer; and

patterning the conducting layer to form the control gate

by using the capping layer as an etching mask.

[c6] 14. The method of claim 9, wherein forming the pocket well of the second conductivity type comprises performing a pocket implantation.

[c7] 15. The method of claim 9, further comprising forming a dielectric spacer on another sidewall of the control gate.

[c8] 16. The method of claim 9, wherein the tunnel oxide is formed by conducting a thermal oxidation process.

[c9] 17. The method of claim 9, wherein the floating gate comprises a doped polysilicon layer.

[c10] 18. The method of claim 9, wherein the capping layer comprises an oxide layer.

[c11] 19. The method of claim 9, wherein the control gate comprises a doped polysilicon layer.

[c12] 20. A method for operating a split gate flash memory cell, wherein the split gate flash memory cell comprises a substrate, a deep n-type well in the substrate, a shallow p-type well in the deep n-well, a gate oxide layer on the shallow p-type well, a control gate on the gate oxide layer, a capping layer on the control gate, a floating gate on a first sidewall of the control gate and the capping layer and over a portion of the substrate, a tunnel oxide

layer between the control gate and the floating gate and between the floating gate and the substrate, a dielectric spacer on the other sidewall of the capping layer and the control gate, a drain in the shallow p-type well and adjacent to the control gate, a common source located in the deep n-type well and extending to the substrate under a portion of the floating gate, and a pocket p-well located in the substrate around the drain and electrically connecting with the shallow p-type well, the method comprising:

during a programming operation, applying a first voltage to the control gate, applying a second voltage to the common source and grounding the drain and the pocket p-well to cause source side injection;

during an erase operation, applying a third voltage to the control gate to eject electrons from the floating gate to the control gate by Fowler-Nordheim tunneling; and

during an reading operation, applying V_{cc} to the control gate, applying a forth voltage to the drain and grounding the common source and the pocket p-well.

[c13] 21. The method of claim 20, wherein the erase operation comprises:

applying a positive voltage to the control gate, applying a negative voltage to the common source and floating the drain and the pocket p-well to cause Fowler-

Nordheim tunneling for erasing.

[c14] 22. The method of claim 21, wherein the positive voltage is about 12V and the negative voltage is about 8V.

[c15] 23. The method of claim 20, wherein the first voltage is about 2V and the second voltage is about 10V.

[c16] 24. The method of claim 20, wherein the third voltage is about 20V.

[c17] 25 The method of claim 20, wherein the forth voltage is about 1.5V.